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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 27/102, 29/41, 29/735

A1

(11) International Publication Number: **WO 00/35018**

(43) International Publication Date: 15 June 2000 (15.06.00)

(21) International Application Number: PCT/US99/29263

(22) International Filing Date: 10 December 1999 (10.12.99)

(30) Priority Data:
60/111,972 11 December 1998 (11.12.98) US

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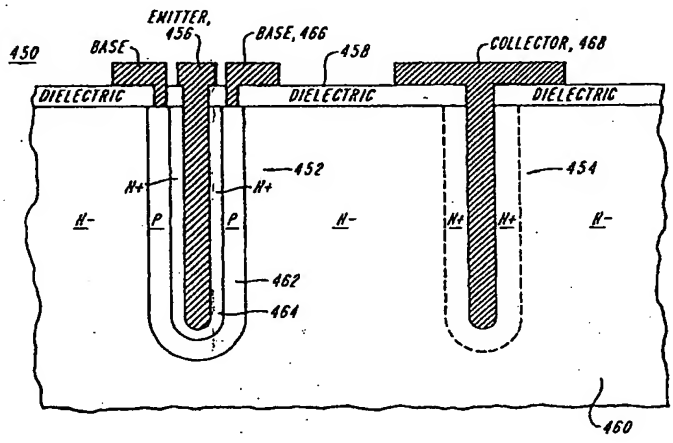
(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: SIDEWALL JUNCTION FOR BIPOLAR SEMICONDUCTOR DEVICES



(57) Abstract

A bipolar semiconductor device (450) having sidewall junction structures is comprised of a wafer substrate (460) having substantially vertical trenches (452, 454) formed therein and defined by a plurality of sidewalls. Through the sidewalls, dopants of preselected conductivity are introduced into the substrate to form sidewall junctions (462, 464). Additionally, the vertical trenches are used to contain a corresponding metal electrode (456, 468) (e.g., emitter, collector cathode, or anode) of the device, such electrodes being a function of the type of semiconductor junction device formed. According to the present invention, the current flow is parallel to the wafer surface (458), as with a typical lateral device, but the current flow is also perpendicular to the surfaces (i.e., sidewalls) through which the dopants are introduced, which is typical of a vertical device. Such a sidewall junction structure results in better utilization of the area volume of the device. Semiconductor junction devices which may be formed using the present invention include transitors, thyristors, and rectifiers.

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SIDEWALL JUNCTION FOR BIPOLAR SEMICONDUCTOR DEVICES

FIELD OF THE INVENTION

The invention relates to semiconductor devices generally, and more specifically to the junction structures of such semiconductor devices.

BACKGROUND OF THE INVENTION

Typical bipolar semiconductor devices (e.g., transistors, thyristors, and rectifiers) include junction structures which are either lateral or vertical. In either case, the wafer (e.g., silicon wafer) which forms a substantive portion of the device is doped from a top side and, sometimes, from an opposite bottom side. Vertical and lateral structures for bipolar transistors and thyristors are well known, and have been used for many years. Figures 1A-B show examples of typical prior art vertical and lateral NPN bipolar transistors 10 and 30, respectively. Figures 2A-B show prior art vertical and lateral unidirectional thyristors 50 and 70, respectively. Figures 3A-B show cross sections through two prior art vertical bidirectional thyristors 90 and 100, respectively. Although lateral thyristors are sometimes used in integrated circuits where the process does not permit a vertical device, they are seldom used in discrete devices because they are much less efficient than vertical devices in terms of utilization of area and volume.

Thyristors may be made with or without a gate electrode (e.g., gate 72 in Figure 2B), but in either case, the active area structure is essentially the same. Without the gate electrode, as in Figure 3B, such thyristors would be triggered by some other means, such as by a voltage, dV/dt, or light, and might include a structure to facilitate such triggering. Without the gate electrode, thyristors are known as unidirectional or bidirectional diode (2 terminal) thyristors. With the gate electrode, thyristors are known as unidirectional or bidirectional triode (3 terminal) thyristors, such as those shown at 50, 70, and 90. Unidirectional triode thyristors are also known as semiconductor controlled rectifiers (SCRs), and bidirectional triode thyristors are also known as triode alternating current (AC) switches (TRIACSs).

As can be appreciated when comparing Figures 2A-B and 3A-B, bidirectional thyristors are really two unidirectional thyristors, built side by side into a single chip, one

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with an N emitter (N+) 92 on top, the other with an N emitter 98 on the bottom. To manufacture these types of thyristors, it is required that both N+ and P+ areas on both the top surface A and the bottom surface B of the chip or wafer be formed. Therefore, photomasking is required on both surfaces of the wafer. During the manufacturing process, such wafers are susceptible to breakage because they are thin and relatively fragile. Even with the thinnest wafers which can be manufactured, the wafers are much thicker than would be required for optimum performance.

In all of the above prior art structures, the dopants which form the junctions are diffused into a substrate from the wafer surface or surfaces, such as substrate 95 and surfaces A and B in Figure 3A. In the vertical structures (e.g., transistor 10), current flow is perpendicular to the surface from which the wafer is doped, as shown in Figure 1A. In the lateral structures (e.g., transistor 30), current flow is substantially parallel to the surface from which the wafer is doped, as shown in Figure 1B. Such devices leave a great deal of volume unused, so inherently limit the number of devices which can be included in a given substrate volume. In order to more efficiently utilize the area and volume, or reduce the required volume, of such devices, a structure which is like the lateral device in that the current flow is parallel to the wafer surface, but which is like the vertical device in that the current flow is perpendicular to the surfaces through which the dopants were introduced would be advantageous.

In addition, thyristors usually contain emitter shunt resistors to stabilize the device's triggering characteristics. These shunt resistors allow any current, such as thermal leakage current, dV/dt displacement current, avalanche current, or gate current, to bypass the emitter junction until the drop on the resistor reaches around 0.7 volts. At this voltage, emitter current rises rapidly and switches the device on. This resistor holds the triggering current in a narrow range, over a wide range of variations in the individual transistor gains. In the prior art thyristor structures, shown in Figures 2A-B and 3A-B, the emitter shunt resistor consists of the lateral resistance of the P base beneath the N emitter, connected to the cathode metal through an array of shorting dots 54, 96, and 104. Since in the prior art these shorting dots are doped in from the top and/or bottom surfaces of a vertical device, the shorting dots can be readily defined by conventional photo-masking techniques.

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Finally, many circuits require the use of a diode in parallel with the thyristor to permit current to flow when the anode of the thyristor is negative relative to the cathode. A device combining these types of elements on a single chip is known as an integral thyristor rectifier (ITR). In the 1970's, vertical ITRs were sold by the millions. These were 600-volt devices, so their optimum thickness was ideally around 60 microns, but because of wafer breakage problems, ITRs were made on 150 micron wafers and could therefore not achieve optimum performance. ITRs were eventually abandoned because even at 150 microns there was severe wafer breakage and performance was generally unacceptable at greater thicknesses. It would be advantageous to have ITR devices that could be made with fully optimized anode to cathode spacings, on whatever wafer thickness can be readily manufactured, e.g., for thickness as small as about 600 to 800 microns. However, thicknesses outside of this range may also be useful.

SUMMARY OF THE INVENTION

The present invention is a sidewall junction structure as part of a semiconductor device. The device is comprised of a wafer which defines a substrate having substantially vertical trenches formed therein, each trench being defined by at least two opposing sidewalls. Through the sidewalls, dopants of preselected conductivity are introduced into the substrate to form the sidewall junctions. Each vertical trench is then used to contain a corresponding metal electrode (e.g., emitter, collector, cathode, or anode) of the device, such electrodes being a function of the type of semiconductor junction device formed. According to the present invention, the current flow of the device is parallel to a top surface of the wafer, as with a typical lateral device, but the current flow is also perpendicular to the surfaces (i.e., sidewalls) through which the dopants are introduced, which is typical of a vertical device. Such a configuration allows better utilization of the area and volume of the device. Semiconductor junction devices which may be formed using the present invention include, for example, transistors, thyristors, and rectifiers.

In one embodiment, an NPN bipolar transistor is formed using a P-type base substrate, within which at least two trenches are etched. The sidewalls of the trenches are then doped with an N emitter (i.e., N+) dopant and an emitter electrode and a corresponding collector electrode are positioned within corresponding trenches. In a different NPN bipolar transistor

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embodiment, at least two trenches are etched into an N– collector substrate, and the sidewalls of a first one of the trenches is doped with a P-type dopant. Then, the sidewalls of each trench are doped with an N+ dopant, wherein a P-type layer is maintained between the N+ dopant layer and the N– collector substrate in the first trench. In this embodiment, an electrically isolated base contact may be coupled to the P-type layer.

In another embodiment, sidewall junctions are formed in a thyristor, wherein a first trench is formed in an N– substrate and doped with a P base dopant initially and then an N+ dopant. The second trench is doped with a P+ dopant. The first trench holds a cathode and the second trench holds an anode. The substrate (or wafer) within which the trenches are etched may be a bulk N– wafer, or an epitaxial N– layer built on an N+ or P+ substrate. The device may be given an N+ gate electrode for turning the device on and off.

Various embodiments of bidirectional thyristors are formed having both N and P emitters formed in the sidewalls of two vertical trenches. Preferably, each embodiment of the bidirectional thyristor, includes a short or shorts to stabilize the triggering characteristics of the device. In one such embodiment, in each trench, an N and a P emitter region is formed in different sidewalls within the same trench, having an emitter dividing line running the length of the trench. To achieve a short, N emitter material may be omitted from the bottom of the trench. In another embodiment, the dividing line runs across the trenches. In this embodiment, the P emitter region also inherently serves as a short. In yet another embodiment, N and P emitter trenches are contained in separate trenches. To form shorts in this embodiment, the P base material may be located close enough to the P+ emitter material so that they contact. Otherwise, shorts may be made by excluding N emitter material from some region of its trench.

Where the bottom of the trenches of a transistor or thyristor are curved, an increased field may be realized in the bottom curved area. This curvature results in a breakdown voltage in that region which is lower than the breakdown voltage at the sidewalls, which is undesirable. Ideally, the breakdown voltage would be the same in both areas and is tuned to the device requirements. The electric field around the curved region may be reduced in a variety of ways. For example, a lower dopant concentration may be used in the region beneath the trenches than is used in the region between the trenches. As a result, at any given voltage the depletion region spreads further downward than sideward. Another way to reduce

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the field at the curved region of a trench is to connect the base region of a junction to a base substrate. In yet another embodiment, a lower field may be achieved by depositing an isolating layer (e.g., an oxide layer) at the bottom of the cathode trench, such that the emitter layer does not contact the base layer in the curved bottom region of the trench.

In an NPN device, for example, if the P base portion of the trench of a thyristor is directly connected to the P base substrate, the substrate may be used as a gate to turn the device on and off. In such a case, it may be desirable to also have shorting P+ contacts along the tops of a cathode trench because the top of the trench will be the last place within the device to turn off, since the signal is coming from the substrate at the bottom of the device. Another way to form emitter shorts along the tops of the trenches would be to exclude the emitter deposition from a strip along the top of the sidewalls of each trench, for example. In such a case, a P+ deposition can be made in that strip.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects of this invention, the various features thereof, as well as the invention itself, may be more fully understood from the following description, when read together with the accompanying drawings, described below.

Figures 1A and 1B are cross-sectional views of prior art vertical and lateral junction structures of NPN bipolar transistors, respectively.

Figures 2A and 2B are cross-sectional views of prior art vertical and lateral junction structures of unidirectional gated thyristors, respectively.

Figures 3A and 3B are cross-sectional views of prior art vertical bidirectional thyristors.

Figures 4A and 4B are cross-sectional views of two embodiments of NPN bipolar transistors with sidewall junction structures, in accordance with the present invention.

Figure 5A is a cross-sectional view of another embodiment of a sidewall junction structure thyristor and Figures 5B-D show various corresponding substrate embodiments, in accordance with the present invention.

Figure 6 is a perspective view of a bidirectional thyristor with N and P emitters split along the length of the trenches, in accordance with one embodiment of the present invention.

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Figure 7 is a is a perspective view of a bidirectional thyristor with N and P emitters split across trenches, in accordance with another embodiment of the present invention.

Figure 8 is a perspective view of a bidirectional thyristor with N and P emitters in separate adjacent trenches, in accordance with yet another embodiment of the present invention.

Figures 9A and 9B are cross-sectional views of two embodiments of NPN bipolar transistors which reduce breakdown voltage around the curved trench bottoms, in accordance with the present invention.

Figures 10 A-D are cross-sectional views of four embodiments of bipolar transistors with substrate base electrodes and which also reduce breakdown voltage around the curved trench bottoms, in accordance with the present invention.

Figures 11 A-D are cross-sectional views of bipolar transistors with substrate gate electrodes and which also reduce breakdown voltage around the curved trench bottoms, in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is a sidewall junction structure as part of a bipolar semiconductor device (e.g., a transistor, thyristor, or rectifier), comprising a wafer defining a substrate, the substrate having substantially vertical trenches formed therein and defined by a plurality of sidewalls. The trenches are used to introduce dopants into the substrate, and to contain the metal of the main current-carrying electrodes of the device. A semiconductor device incorporating the present invention includes some aspects of a lateral device and other aspects of a vertical device. For example, the current flow of the device is parallel to a top surface of the wafer, similar to a typical lateral device, and the current flow is also perpendicular to the surfaces through which the dopants are introduced (i.e., trench sidewalls), similar to the flow in a vertical device. Because the trenches make use of previously unused volumes of the substrate, the present invention yields a more compact device, which typically results in better device performance (e.g., faster switching). That is, the spacing of the device is a function of the distance between corresponding trenches, rather than the thickness of the wafer.

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Figures 4A and 4B show examples of NPN bipolar transistors 400 and 450 respectively, each made with a sidewall junction structure in accordance with the present invention. In each figure, only one emitter trench, 402 and 452 respectively, and one collector trench, 404 and 454 respectively, are shown. For higher current devices, multiple trenches may be connected to the emitter electrode, and a corresponding multiple trenches may be connected to the collector electrode. The trenches connected to the emitter electrode are arranged with respect to the trenches connected to the collector electrode in an alternating manner across the surface of the device, so as to be properly spaced and isolated from one another. In such a case, the emitter and collector electrodes on the top surface would be interdigited, similar in appearance to the emitter and base electrodes of many typical prior art transistors, but with enough separation between them to support the full collector voltage of the device. In each of the preferred embodiments, a dielectric is disposed on the top surface of the wafer, electrically isolating the electrodes from the top surface, e.g., isolating top surface 408 in Figure 4A from substrate 410.

The NPN semiconductor device 400 of Figure 4A comprises a wafer having a P-type substrate 410. Trenches 402 and 404 are etched into substrate 410 from top surface 408 to help form a sidewall junction structure in accordance with the present invention. Trench 402 is an emitter trench having sidewalls doped with an N emitter (N+) dopant and houses an emitter electrode 406. A corresponding collector trench 404 is doped with an N+ dopant to form a dopant layer and houses a collector electrode 412. The N+ sidewalls of each trench along with the P-type substrate between the trenches, forms an NPN transistor device 400. The substrate 410 into which the trenches are etched serves as the base region of the device and could be, for example, a P-type float zone or Czochralski wafer, or a P-type epitaxial layer on a P+ substrate wafer.

In the semiconductor device 450 of Figure 4B, the junction structure includes trenches 452 and 454 etched into an N-type substrate 460, rather than a P-type substrate as in Figure 4A. That is, substrate 460 is to be of the same conductivity type as the emitter and collector. In this embodiment, base regions are formed by depositing a P-type base dopant 462 onto the sidewalls of the emitter trench 452 and diffusing the P-type dopant into the sidewalls. An N+ dopant is deposited over base region 462 to form an N emitter dopant layer 464. An emitter electrode 456 is created within emitter trench 452 and a base electrode is electrically coupled

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to base dopant layer 462 through top surface 458. Additionally, an N+ dopant is diffused into the sidewalls of collector trench 454, which houses collector electrode 468. In this structure, in operation the substrate is at collector potential, rather than base potential, and can be used to carry part or all of the collector current. Generally, to reduce resistance, the collector trenches could be etched deeper than the emitter trenches, and could extend to an N+ region or layer of the substrate, if the substrate also included such a layer. In the devices of Figures 4A and 4B, the wafers 410 and 460 are shown as bulk substrates of P- and N– conductivity, respectively.

As is apparent from the devices of Figures 4A and B, a significant advantage of devices structured in accordance with the present invention is that the sidewall junction structure greatly increases the active volume of the semiconductor material per unit of wafer area from what is possible with the prior art lateral or vertical structures. In the prior art lateral structures, the active volume extends only slightly beyond the depth of the diffusions which form the active area of the device. In the prior art vertical structures, the active volume of the device can extend through the full thickness of the wafer, but only if the thickness of the wafer is small enough to match the voltage at which the device is designed to operate. The maximum thickness which can be considered to be active volume is the upper base thickness plus the thickness of the voltage-supporting region beneath the upper base, such as the N+ region 562 in Figure 5C. In silicon, for each 10 volts of operating voltage, the device needs only approximately one micron of thickness. Wafer thicknesses are usually well over the minimum needed (e.g., about 200 microns), in order to make them strong enough for relatively reliable handling and manufacturing.

In contrast, semiconductor devices having sidewall junction structures in accordance with the present invention have active volumes that may extend down to the depth of the trenches, and may be as thin as about 5 microns. The inventive sidewall junction structure is in effect somewhat like many thin vertical devices, which are active through their entire thickness, stacked one on top of another, then rotated 90 degrees and placed orthogonally on edge on a handle wafer. Instead of making the vertical devices separately and stacking them, the semiconductor devices of the present invention are made by cutting or etching grooves or trenches into a wafer, with the separation between the trenches being chosen as a function of

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the operating voltage of the device, and then forming the active junctions on the sidewalls of the trenches.

The sidewall junction structure of the present invention also achieves an improved passivation system, i.e. the system to make the transition from supporting the voltage in the wafer (e.g., silicon) to supporting the voltage in the environment without producing arcing, leakage currents, or unstable breakdown. In both lateral and vertical prior art structures, the high voltage junctions are parallel to the top surface and must be curved upward to bring the junctions to the top surface where they can be passivated. This upward curvature of the junctions causes an increased electric field, so the junctions must be surrounded with various structures, such as field limiting rings and field plates, in order to avoid avalanche breakdown near the surface dielectrics, where such avalanche-generated carriers could charge the dielectrics and cause unstable breakdown characteristics. In a device having the sidewall junction structures of the present invention, the high voltage junctions are perpendicular to the top surface, so they intersect the top surface with no curvature and no increased electric field. A simple field plate, comprising metal extending over the dielectric a slight distance beyond the junction is sufficient to prevent surface breakdown. In this way, each high voltage electrode is its own high voltage passivation system, with no need for a ring of edge passivation surrounding the entire die. Any junction curvature is buried deep below the surface in the substrate, where avalanche-generated carriers can not be trapped on dielectrics.

The advantages of the sidewall junction structure may be even greater for thyristors than for transistors. Figure 5A shows a sidewall junction structure 500, that can be adapted and used to make a unidirectional or a bidirectional thyristor. Structure 500 is similar to the structure of the NPN transistor 450 of Figure 4B except that the N+ collector trench 404 of Figure 4B has been replaced with a P+ emitter trench 504 in Figure 5A, which becomes the anode region of the thyristor and houses anode 514. The cathode trench 502 of thyristor 500 includes a P-type base region 506 doped into the sidewalls of emitter trench 502. Then, trench 502 is doped with an N+ conductivity material to form an N+ dopant layer 508 and cathode 512 is housed therein. The wafer 510 into which the junction is built is shown as a bulk substrate of N– conductivity (also shown in Figure 5B), but could alternatively be an epitaxial N- layer on either an N+ substrate layer 562 or P+ substrate layer 572, as shown in Figures 5C and 5D respectively.

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To construct a gated thyristor, a gate similar to the P base contact 466 of Figure 4B may be attached to the P base region 506 of device 500 somewhere within the junction area, thereby forming a gate electrode which would turn the device on when given a positive bias with respect to the cathode. The N+ substrate layer 562 electrode of Figure 5C could also serve as a gate. The gate formed would be an N-type base gate, which would turn the device on when given a negative bias with respect to the anode. This substrate electrode 516 could also serve as a collector to allow the device to function as a vertical NPN device. The gate formed could also be used as a turn-off device. That is, if a positive bias is applied to such a gate, electrons from the N emitter 508 are diverted downward, causing the P emitter 504 to lose its forward bias, thereby stopping hole injection and allowing the device to switch off. When built on a P+ substrate layer, as in Figure 5D, the substrate could be used as an anode region for vertical thyristor type of conduction. If the device is to be a non-gated, or diode, thyristor, the active area would appear as shown in Figure 5A. If the device does not include a substrate gate, there is no need for a current-contact 516 on the back of the wafer (shown in Figures 5B, 5C, and 5D), since all of the current would flow through the top-surface electrodes, and the back contact 516 would serve as primarily a means for heat removal if included.

Figures 6, 7, and 8 show some possible configurations for the emitter areas of a bidirectional thyristor made with different sidewall junction structure embodiments, in accordance with the present invention. As noted above, a bidirectional thyristor requires both N and P emitter areas on each of the two current-carrying electrodes. In Figure 6, a thyristor 600 having a plurality of similar trench pairs formed in an N-type substrate 604 is shown. Each emitter trench, e.g., trench 602, has an N emitter doped region 606 and a P emitter doped region 608 formed along its length, with one sidewall being an N emitter dopant layer and the other being a P emitter dopant layer. A first electrode 610 is housed within trench 602 and serves as a cathode. A second electrode, i.e., an anode 614, is housed within a corresponding trench 612. With the device of Figure 6, as with prior art thyristors, it is important to stabilize the triggering characteristics of the device. However, shorting dots like those used with respect to the prior art devices of Figures 2A-B and 3A-B, which are formed by suitably masking the top surface of each device, do not lend themselves to the trench structure of the present invention. One way to form shorting contacts in the devices having

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sidewall junction structures in accordance with the present invention is to exclude the N+ material from the top edge and/or bottom edge of the trenches. With respect to the device of Figure 6, having the N emitter excluded from one sidewall of each trench 602 and 612, thyristor 600 inherently has a short along the bottom edge of every N emitter.

Figure 7 shows an alternative embodiment of a bidirectional thyristor 700 having sidewall junctions with N and P emitters split across the trenches. Thyristor 700 has a plurality of trench pairs formed within a N-type substrate 704, each trench having alternating vertical sections of P emitter dopant layer and N emitter dopant layer vertically disposed along its length. In the preferred forms each sidewall of each trench is substantially a mirror image of its opposing sidewall. The N emitter region or layer is separated from substrate 704 by a P-type region or layer doped into the sidewall prior to doping in the N emitter dopant. Trench 702 houses a first electrode, i.e., cathode 710, which contacts both P and N emitter regions within the sidewalls of the trench. A corresponding second electrode, i.e., anode 714, is similarly housed within trench 712 and contacts both of the P and N emitter regions of that trench. This sidewall junction structure forms an inherent shunt by excluding the N emitter 706 from the trench sidewall along portions of the length of the trench. The P+ regions 708 serve both as emitters and shunt resistors, with the value of the shunt resistor depending on the widths of the N emitter regions.

Yet another embodiment of a bidirectional transistor having sidewall junctions and emitters split across the trenches is thyristor 800 shown in Figure 8. In thyristor 800, the N emitters and P emitters are contained in separate sub-trenches etched in an N-type substrate 804 that together alternatively form either a cathode or anode trench. The sub-trenches are elongated trenches that extend lengthwise along a common axis. As an example, sub-trenches 806 and 812 collectively may be used as a cathode trench 802. In such a case, an electrode 810 serves as a cathode and has a first portion housed within N emitter sub-trench 806 and a second portion housed within P emitter sub-trench 812, as shown with trench 802. Accordingly, sub-trenches 808 and 818 serve as an anode trench 816 and house a first and a second portion of an electrode, i.e., anode, 814. If the ends of trenches 802 and 808 are close enough for P base and P emitter to meet, as shown, the P emitters can still function as N emitter shorting contacts. If trenches 818 and 808 are too far apart for the P regions to meet, the shorting contacts must be made by excluding N emitter from some region of its trench,

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such as the top edge, bottom edge, or end-walls. Preferably, as shown in Figure 8, the P regions of the sub-trenches do meet and shorting contacts are formed.

Each of the sidewall junction structure embodiments shown in Figures 6, 7, and 8 eliminates some inherent manufacturing problems of the prior art, because thyristors 600, 700, and 800 require photo-masking on only one side of the wafer, can have whatever emitter and base widths are needed for optimum performance, and can be made on any thickness of wafer without degradation of performance. Various factors will enter into the choice of the emitter configuration. One factor might be the type of etching, masking, and dopant deposition systems available for the manufacture of the device. Another factor might be electrical specifications of the device, such as on-voltage and commutating dV/dt (CdV/dt) (the ability of the device to withstand a dV/dt in one direction immediately after it has been conducting in the other). CdV/dt would probably be higher with the device of Figure 6, because in thyristor 600 the conduction takes place between every other pair of trenches, giving greater separation between the carriers left over from conduction in one direction and the region which is susceptible to being turned on in the opposite direction. With thyristors 700 and 800 of Figures 7 and 8, respectively, conduction occurs between all trenches for both directions of bias, which may result in a lower CdV/dt capability, but should also result in a lower on-voltage for these devices. The lowest possible on-voltage is always desirable, but whether it is better to have a low or a high CdV/dt depends on the application. High CdV/dt is desirable for high frequency (e.g., 400 Hz) phase control applications, while low CdV/dt is desirable for bidirectional surge suppression applications.

In the structures shown in Figures 4A-8, junction curvature around the bottom of a trench will cause the breakdown voltage in that area to be lower than the breakdown voltage is in the area near or between the sidewalls, which is typically considered undesirable. To address such occurrences, measures may be taken to reduce the electric field around this curvature at or near the bottoms of the trenches. The optimum dopant concentration for the N- region between trenches is that concentration which (on a non-curved junction) produces an avalanche breakdown voltage just over the rated voltage of the device. The optimum width for this region is a width just over the depletion width at which breakdown occurs. A width greater than this will add series resistance, and a width less than this will reduce breakdown voltage.

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Figures 9A and 9B show two embodiments of semiconductor junction devices, 900 and 950, respectively, having electric field-reducing structures at the bottom of the trenches. In each of these embodiments, a lower dopant concentration is used in the region beneath and adjacent to the trenches than the dopant concentration between the trenches, so that at any given voltage, the depletion region spreads further downward than it spreads sideward. Referring to device 900 of Figure 9A, two trenches are etched into an N-type substrate, cathode trench 920 and anode trench 922. In each trench, a lightly doped N-type region 904 is formed after trench etching but before the P base deposition 906, by implanting a low dose (on the order of about 1E12/cm^2 to 1E13/cm^2) of P-type dopant into the trench bottoms and diffusing it in to the sidewalls to counter-dope and reduce the N-type dopant concentration in the regions beneath the trenches. Next, trenches 920 and 922 are generally formed as described with respect to Figures 4B and 5, for example. That is, the sidewalls and bottom of trench 920 are doped with a P-type material and then an N emitter material and electrode 916 is housed within trench 920. The sidewalls and bottom of trench 922 are doped with a P emitter material and electrode 912 is housed therein. As with previous embodiments, dielectric 918 insulates substrate 902 from electrodes 912 and 916.

Referring to the semiconductor device 950 of Figure 9B, a lightly doped N-type region 954 is formed as part of substrate 952 before trench etching. In the preferred form, the wafer or substrate is formed by depositing an epitaxial N– base layer 956 on the more lightly doped N-- substrate wafer 954. A cathode trench 968 and an anode trench 970 are then etched into the wafer such that the curved part of each trench is located in the more lightly doped N-- region or layer 954. N layer 954 contains the curved regions of trenches 968 and 970 and thereby reduces the electrical field in those regions, for reasons previously stated. As with the previous thyristor embodiments, cathode trench 968 is first doped with a P-type of dopant 962 and then with an N emitter dopant to form N+ dopant layer 964. Also, as with previous thyristor embodiments, the anode trench 970 is doped with a P emitter dopant to form P+ dopant layer 958. Cathode 966 and anode 960 are then housed within their respective trenches, 968 and 970.

With either of thyristor 900 or 950, the N-- and N- regions or layers can be selectively chosen to have a dopant concentration low enough to produce a trench-bottom breakdown voltage which is less than, equal to, or greater than the breakdown voltage between trenches.

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These methods and structures for reducing the electric field around the curvature at the trench bottoms are, of course, applicable to transistors as well as to thyristors.

When forming diode thyristors, which are typically specified to have a breakover voltage within a tightly controlled range, some consideration must be given to the inclusion of a tightly controlled breakdown region within the structure. This may be accomplished by implanting an N-type layer on the top surface to reduce the breakdown voltage there. However, since breakdown at the surface can charge dielectrics and cause breakdown to change, it would be preferable to keep the breakdown structure further from the top surface. One approach to controlling the breakdown away from the top surface is to control the dopant concentration and curvature of the trenches closely enough to achieve the specified voltage. Another approach is to epitaxially grow the N- layer with a tightly controlled, more heavily doped N layer in it, below the surface. Yet another approach is to implant such a heavily doped N-type layer into the substrate, although this might require a very high energy implant.

In bipolar semiconductor transistors having sidewall junction structures similar to that of Figure 4B and having a P-type base region 462 formed in trench 452, the base contact must be made somewhere on the top surface, and may require some fairly small geometries to make the contacts. Additionally, forming the base contact may require double layer metal to distribute the base metal over the surface without interfering with the emitter and collector metal. One approach to avoiding the difficulty involved with forming such a base contact with the structure of Figure 4B is to bring the base electrode 466 through the substrate 460, rather than through the top surface 458. If desired, the device of Figure 4A could have a base electrode (not shown) on substrate 460, but at the penalty of having a base region (i.e., P-type region 410) which is much wider than the diffused base of device 450 of Figure 4B, and with the voltage supported in the base rather than in the collector region, which is generally undesirable. Therefore, in some circumstances it would be advantageous for devices to have a diffused base structure.

Figures 10A-10D show bipolar semiconductor devices (i.e., transistors) having various sidewall junction structure embodiments. Each embodiment includes a layered substrate having a base electrode 1006, forming a diffused-base structure. In Figure 10A, a semiconductor device 1000 is shown having an N- epitaxial layer 1004 built on a P+ substrate 1002. An emitter trench 1014 (housing emitter electrode 1008) and a collector trench 1012

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(housing collector electrode 1010) are etched into an N- substrate layer 1004, wherein a P doped base region 1018 of trench 1014 is etched significantly deeper than collector trench 1012 so that the P base diffusion region 1018 meets P+ substrate layer 1002 and the collector trench is sufficiently isolated from the base diffusion region (i.e., layer 1002). This structure allows P+ substrate layer 1002 to be used as a base contact between base electrode 1006 and P base region 1018. Additionally, the N emitter layer 1016 of trench 1014 does not intersect P+ layer 1002 (this would short the emitter). An added advantage to the structure of device 1000 is that this effectively changes the direction of junction curvature at the trench bottom, since the bottom of trench 1014 is subsumed within P+ layer 1002, leaving almost no curvature in N- substrate layer 1004. Accordingly, the electrical field near the trench bottom is reduced, rather than increased, and breakdown much less likely to occur in that region.

Furthermore, the sidewall junction structure of device 1000 offers potential advantages in gain over the device of Figures 4A-B. The gain of device 1000 is higher than that of device 400, due to the thinner base region of device 1000. The gain of device 1000 would also be higher than that of device 450 because the emitter and base current both enter from the top surface 458 in device 450, so any IR drops tend to accumulate and progressively de-bias emitter 456, causing an undesirable fall-off in current density toward the bottom of the device, thus reducing the gain. When the base current comes in from the bottom and the emitter current from the top, as in the devices of Figures 10A-D, IR drops tend to cancel out and produce uniform injection over the entire emitter area.

Semiconductor device 1030 of Figure 10B is another embodiment of a sidewall junction structure, which also places a base electrode 1052 on a substrate. However, in this embodiment emitter trench 1032 and collector trench 1034 have the same depth. In the preferred embodiment, this is accomplished by beginning with a P+ substrate 1036 onto which a P- layer 1038 is deposited. Next, an N- layer 1040 is deposited on P- layer 1038. Trenches 1032 and 1034 are then etched to a depth slightly less than the N-/P- junction and the P base 1046, N+ emitter 1048, and N+ collector regions are formed by doping the sidewalls of trenches 1032 and 1034, as described with respect to previous embodiments. Emitter electrode 1050 is housed within emitter trench 1032 and collector electrode 1044 is housed within collector trench 1034. The N-/P- junction produces a sufficiently wide depletion region to reduce the electric field beneath both trenches. Even though it is only

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lightly doped, P- region 1038 still has adequate conductivity to allow the substrate to act as a base electrode (or at least a conductive path to base electrode 1052 via P+ layer 1036), since base current is small compared to emitter-collector current. P- layer 1038 may also serve as a base ballast resistance to assure a uniform distribution of base current by preventing the base current from focusing into hot spots.

In either of the structures of the devices shown in Figures 10A-B, collection of the carriers injected from the bottoms of the trenches may be less efficient than collection of carriers injected from the sidewalls, because of the greater distance the carriers from the bottom must travel to reach the collector region. For this reason, it may be desirable to eliminate the emitter dopant and the emitter contact from the bottoms of the trenches. This may be accomplished by depositing oxide in the bottoms of the emitter trenches prior to the emitter deposition, and leaving the oxide in the trench bottoms to isolate the emitter metal from the base region. Figures 10C-D show the same structures as Figures 10A-B, respectively, but with the bottom emitter excluded and an oxide deposit 1062 and 1082 at the bottom of emitter trenches 1064 and 1084, respectively.

Figures 11A-D show the substrate-base-electrode concept applied to a thyristor, constructed in a similar manner as the bipolar transistors of Figures 10A-D, therefore, each device has at least one cathode trench and one anode trench. Thyristors 1100, 1130, 1150 and 1170 are shown with bottom emitter exclusions and oxide deposits, but like the transistors of Figures 10A-B, these thyristors could be made with or without oxide deposits. Thyristor 1100 of Figure 11A has a sidewall junction structure which accomplishes blocking, (i.e., the ability to support voltage) in both directions, with the cathode trench 1114 etched deeper than the anode trench 1112 into N– substrate 1104, and a P base region doped into trench 1114 which extends into P+ base layer 1102. Blocking in both directions is achieved by having only trench 1114 intersecting P+ layer 1102, because if both trenches intersected the substrate layer 1102, the P+ substrate would short out the forward and reverse blocking junctions. As with previous thyristor embodiments, trench 1114 is also doped with an N emitter dopant to form N emitter layer 1120 and houses cathode electrode 1108 and anode trench 1112 is doped with a P emitter dopant to form P emitter layer 1116 and houses anode electrode 1110. A conductive path between gate 1106 and P region 1118 is formed by the intersection of P

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region 1118 with P+ substrate layer 1102 and the contact between gate electrode 1106 and layer 1102.

If only forward blocking is required, the semiconductor device can be of the form of thyristor 1130 of Figure 11B, wherein the emitter trench 1132 and collector trench 1134 have the same depth. In this embodiment, a sidewall P-type base layer 1146 intersects a P- substrate layer 1138, and thus is linked to gate 1152 through a P+ substrate layer 1136. A P+ emitter region 1142 is surrounded by a sidewall N-type buffer layer 1144 to separate it from P- region 1138. Such an N-type buffer region is desirable on any device which does not require reverse blocking because it permits the N base layer 1144 thickness to be reduced to close to half of what would be required without this layer. The thinner N base layer 1144 results in lower on-voltage and faster switching for device 1130. Thyristor 1130, incorporating this sidewall junction structure, still has some reverse blocking capability, possibly on the order of 30 volts, but reverse blocking capability is much lower than the forward blocking capability of device 1130. For reasons discussed previously, each trench, 1132 and 1134, has its emitter material extruded from the bottom of the trench and an oxide deposit, 1148 and 1150, occupying these portions of the trench bottoms.

In each of devices 1100 and 1130, since the sidewall P base layer (e.g., base 1118) is directly connected to the P-type substrate layer (e.g., substrate 1102), each P+ substrate layer can serve as a gate, or as a conductive path to a gate electrode such as gate electrode 1106, to turn its device on. Also, with its large area and low resistance connection to the entire device area, the P-type substrate layer may also serve as a very effective turn-off gate. Each P-type substrate can also be connected to its respective cathode through a resistor anywhere on the chip to provide an emitter shunt. If the P-type substrate is used as a turn-off gate, it may be desirable to also have shorting contacts along the tops of the trenches, because the tops will be the last places to turn off when the turn-off signal comes in from the bottom of the device. One way to accomplish this is with the sidewall junction structure of thyristor 1150 shown in Figure 11C, wherein a portion of dielectric 1154 is removed from the top surface edges of cathode trench 1156 so that the cathode metal 1158 makes contact across the emitter-base junction (i.e., N+ emitter 1160 and P+ base region 1152).

Another approach to forming emitter shorts along the top surface of a thyristor is shown with the sidewall junction structure of thyristor 1170 shown in Figure 11D. The

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structure of thyristor 1170 has an emitter deposition excluded from a strip along the top of each trench sidewall. In this embodiment, the thyristor has this type of short on both the cathode trench 1176 and anode trench 1178. In the cathode trench 1176, a P-type short 1172 is formed in the trench sidewall above the N emitter dopant layer 1182. Similarly, in the anode trench 1178, an N-type short 1174 is formed in the trench sidewall above the P emitter dopant layer 1180. A short on the P emitter results in a complete loss of the reverse blocking capability, which is a disadvantage for some applications, but a distinct advantage for others. Many circuits require the use of a diode in parallel with the thyristor to permit current to flow when the anode of the thyristor is negative relative to the cathode. The two emitter shorts shown in Figure 11D provide such a diode, which is monolithically built into thyristor 1170. A device having these types of characteristics generally is known as an integral thyristor rectifier (ITR). Unlike prior art ITRs, using the structure of Figure 11D, such devices may be made with fully optimized anode to cathode (i.e., trench) spacings, on whatever wafer thickness can be readily manufactured. The sidewall junction structure opens up some new possibilities for controlling the reverse recovery characteristics because by varying the dopant concentration, and even the conductivity type, in the vertical direction, it is possible to build in zones with a variety of different charge storage characteristics to direct the device toward a fast or slow, sharp or soft recovery to more closely match the circuit requirements.

The invention may be embodied in other specific forms without departing from the spirit or central characteristics thereof. For example, all of the structure embodiments described and shown herein could alternatively incorporated in complementary (e.g., PNP) devices made by interchanging conductivity types. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appending claims rather than by the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

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What is claimed is:

1. A semiconductor junction device comprising:

a substrate including a material of at least one predetermined conductivity type and at least two vertical trenches formed in the material, each trench including:

(i) opposing sidewalls;

(ii) at least one dopant of a preselected conductivity type disposed in at least one of said sidewalls so as to form at least one dopant layer in said sidewall creating a junction of said device; and

(iii) a conductive electrode disposed in the trench and in electrical contact with the corresponding dopant layer; and

wherein the predetermined and preselected conductivity types are such that when a predetermined potential is applied between the electrodes current flows between said trenches.

2. The semiconductor junction device of Claim 1 wherein said at least two vertical trenches includes a first trench housing a first electrode and a second trench housing a second electrode, wherein said first trench includes:

a first dopant layer of a preselected emitter conductivity; and

a base dopant layer of a preselected base conductivity formed between said substrate and said first dopant layer.

3. The semiconductor junction device of Claim 2 further including a base electrode electrically coupled to said base dopant layer.

4. The semiconductor junction device of Claim 1 wherein the at least two vertical trenches includes a first trench and a second trench, wherein said first trench includes a first dopant layer comprised of an N emitter material.

5. The semiconductor junction device of Claim 4 wherein said second trench includes a second dopant layer comprised of an N emitter material.

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6. The semiconductor junction device of Claim 4 wherein said second trench includes a second dopant layer comprised of a P emitter material.

7. The semiconductor junction device of Claim 1 wherein said substrate is doped with a P- conductivity dopant.

8. The semiconductor junction device of Claim 1 wherein said substrate is doped with an N- conductivity dopant.

9. The semiconductor junction device of Claim 1 wherein the at least two vertical trenches includes a first trench having a first sidewall and a second sidewall and housing a first electrode electrically coupled to said first and second sidewalls, wherein said first trench includes:

(a) a first dopant disposed in said first sidewall; and

(b) a second dopant disposed in said second sidewall, having a different conductivity than said first dopant and creating a junction between said first and second sidewalls.

10. The semiconductor junction device of Claim 9 wherein the at least two trenches further includes a second trench having a third sidewall and a fourth sidewall and housing a second electrode electrically coupled to said third and fourth sidewalls, wherein said second trench includes:

(a) a third dopant disposed in said third sidewall; and

(b) a fourth dopant disposed in said fourth sidewall, having a different conductivity than said third dopant and creating a junction between said third and fourth sidewalls.

11. The semiconductor junction device of Claim 10 wherein:

said substrate is of an N– conductivity type;

said first dopant and said third dopant are each N emitter dopant; and

said second dopant and said fourth dopant are each P emitter dopant.

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12. The semiconductor junction device of Claim 10 wherein:
said substrate is of a P– conductivity type;
said first dopant and said third dopant are P emitter dopant; and
said second dopant and said fourth dopant are N emitter dopant.

13. The semiconductor junction device of Claim 9 further including:
a base dopant layer of a preselected base conductivity, having a conductivity type different from that of said first dopant, and formed between said substrate and said first dopant.

14. The semiconductor junction device of Claim 1, wherein opposing sidewalls include a first sidewall and a second sidewall, and said at least one dopant layer includes:
(a) a first dopant layer doped with an N emitter dopant; and
(b) a second dopant layer doped with a P emitter dopant, wherein said first sidewall includes said first dopant layer and said second dopant layer.

15. The semiconductor junction device of Claim 14 wherein said first vertical trench includes a base dopant layer disposed between said first dopant layer and said substrate.

16. The semiconductor junction device of Claim 14 wherein said at least two trenches include a second trench, substantially the same as said first trench.

17. The semiconductor junction device of Claim 1 wherein the at least two vertical trenches includes a first trench and a second trench, and wherein at least the first vertical trench is comprised of at least a first sub-trench and a second sub-trench, wherein:
said first sub-trench includes a first pair of opposing sidewalls doped with an N emitter dopant; and
said second sub-trench includes a second pair of opposing sidewalls doped with a P emitter dopant.

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18. The semiconductor junction device of Claim 17 wherein said substrate is an N– substrate and said junction device includes a P base dopant layer disposed between in the first opposing sidewalls of said first sub-trench and said substrate.

19. The semiconductor junction device of Claim 17 wherein said substrate is an P- substrate and said junction device includes an N base dopant layer disposed between said first opposing sidewalls and said substrate.

20. The semiconductor junction device of Claim 1 wherein the at least two trenches includes (a) a first vertical trench having a top portion and a bottom portion; and

(b) a second vertical trench having a top portion and a bottom portion; and wherein the dopant concentration disposed within said substrate and adjacent to the bottom portion of each of said first and second trenches is lower than the dopant concentration disposed in the substrate between said first and second trenches.

21. The semiconductor junction device of Claim 20 wherein said substrate includes:

(a) a first substrate layer having a first dopant concentration, including the top portion of said first and second trenches; and

(b) a second substrate layer having a second dopant concentration, substantially including said bottom portion of said first trench, wherein dopant concentration of the second substrate is lower than the dopant concentration of said first substrate layer.

22. The semiconductor junction device of Claim 21 wherein the first substrate region has an N– conductivity and the second substrate region has an N-- conductivity.

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23. The semiconductor junction device of Claim 1 wherein the at least two trenches includes: (a) a first vertical trench having a top portion and a bottom portion and including a first dopant disposed in at least one of said first trench opposing sidewalls to form a first dopant layer, wherein a base dopant layer is disposed between said first dopant layer and said substrate; and

(b) a second vertical trench having a top portion and a bottom portion; and wherein said substrate includes:

(i) a first substrate layer having a first dopant concentration, wherein said first substrate layer includes the top portion of said first and second trenches; and

(ii) a second substrate layer having a second dopant concentration of the same conductivity type as said base dopant layer, wherein said second substrate substantially includes said bottom portion of said first trench.

24. The semiconductor junction device of Claim 23, wherein the second substrate layer is a base contact layer, said device further including:

a third electrode coupled to said base contact layer; and

a conductive path, including said base contact layer, from said base dopant layer to said third electrode.

25. The semiconductor junction device of Claim 24 wherein::

said first trench houses an emitter electrode;

said second trench houses a collector electrode; and

said third electrode is a base electrode.

26. The semiconductor junction device of Claim 23 wherein the first trench includes a void region formed in said bottom portion, wherein said first dopant is not present in said void region.

27. The semiconductor junction device of Claim 26 wherein said void region is filled with an oxide deposit.

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28. The semiconductor junction device of Claim 26 wherein the second trench includes a void region formed in said bottom portion, wherein said second dopant is not present in said void region.

29. The semiconductor junction device of Claim 28 wherein said void region is filled with an oxide deposit.

30. The semiconductor junction device of Claim 23 wherein said substrate further includes:

(c) a third substrate layer disposed between said second substrate layer and said third electrode;

wherein said second substrate layer is lightly doped and said third substrate layer is of the same conductivity type as said second substrate layer and more highly doped than said second substrate layer.

31. The semiconductor junction device of Claim 24 wherein::

said first trench houses a cathode;

said second trench houses an anode; and

said third electrode is a gate electrode.

32. The semiconductor junction device of Claim 23 wherein said first trench houses a first electrode and includes at least one shorting contact of a preselected conductivity type disposed in said top portion of said first trench between said base dopant layer and said first electrode, such that the first electrode is electrically coupled to said first dopant layer and said shorting contact.

33. The semiconductor junction device of Claim 32 wherein said shorting contacts are comprised of an emitter material of a different conductivity type than said first dopant layer.

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34. The semiconductor junction device of Claim 32 wherein said second trench houses a second electrode and includes a second dopant disposed in at least one of said second trench opposing sidewalls to form a second dopant layer, wherein a second base dopant layer is disposed between said second dopant layer and said substrate and at least one shorting contact of a preselected conductivity type is disposed between said second base dopant layer and said second electrode, such that the second electrode is electrically coupled to said second dopant layer and said second shorting contact.

35. The semiconductor junction device of Claim 34 wherein said second shorting contact is comprised of an emitter material of a different conductivity type than said second dopant layer.

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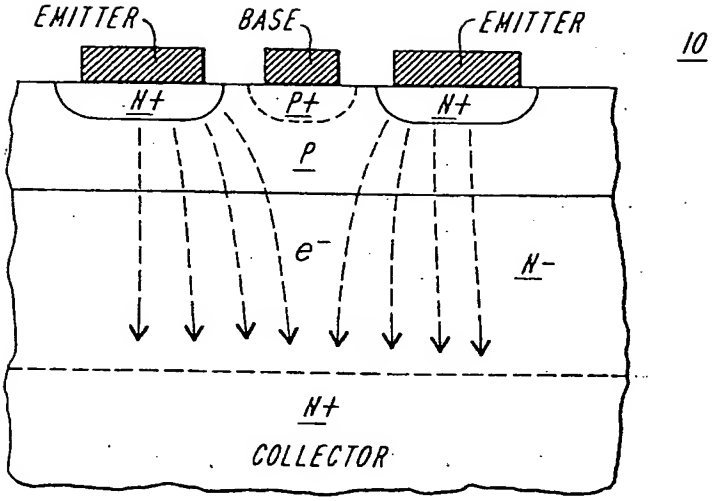

FIG. 1A
(PRIOR ART)

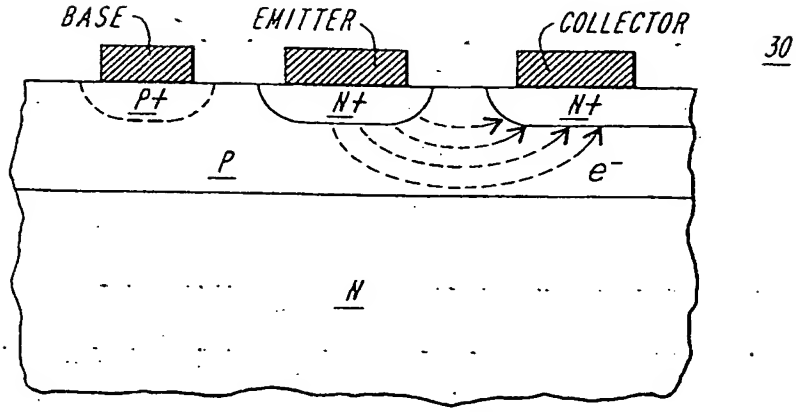

FIG. 1B
(PRIOR ART)

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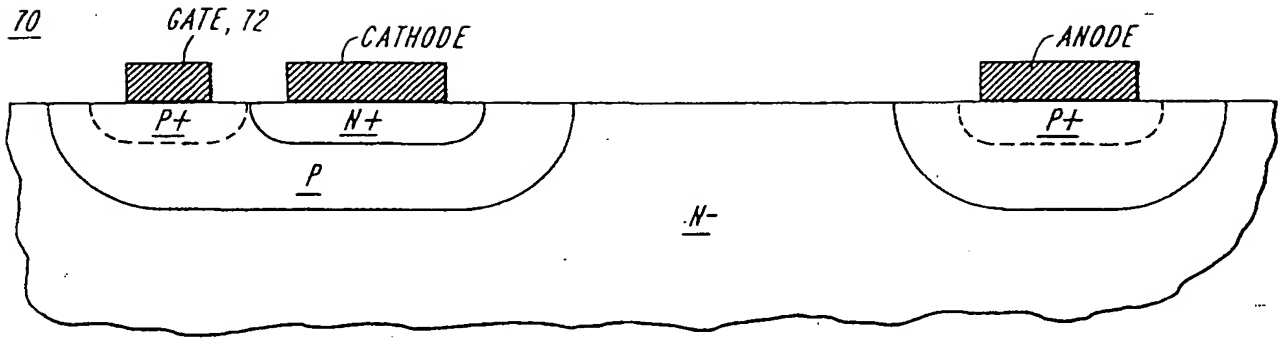

FIG. 2B
(PRIOR ART)

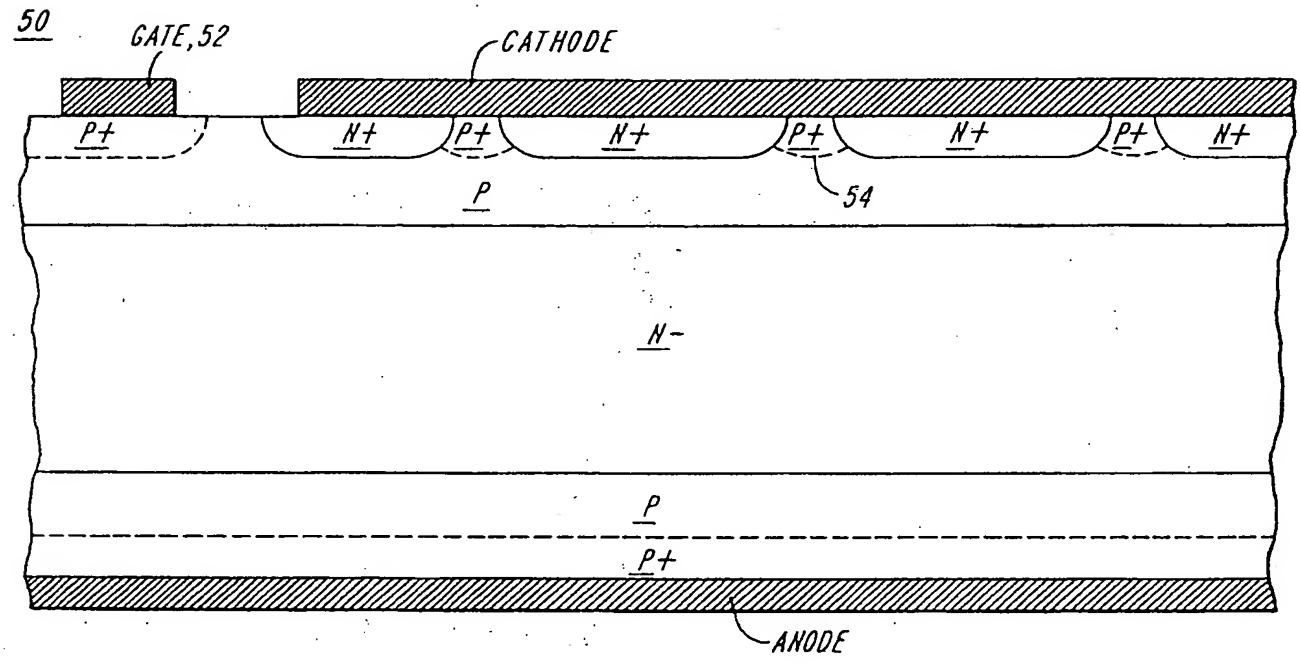

FIG. 2A
(PRIOR ART)

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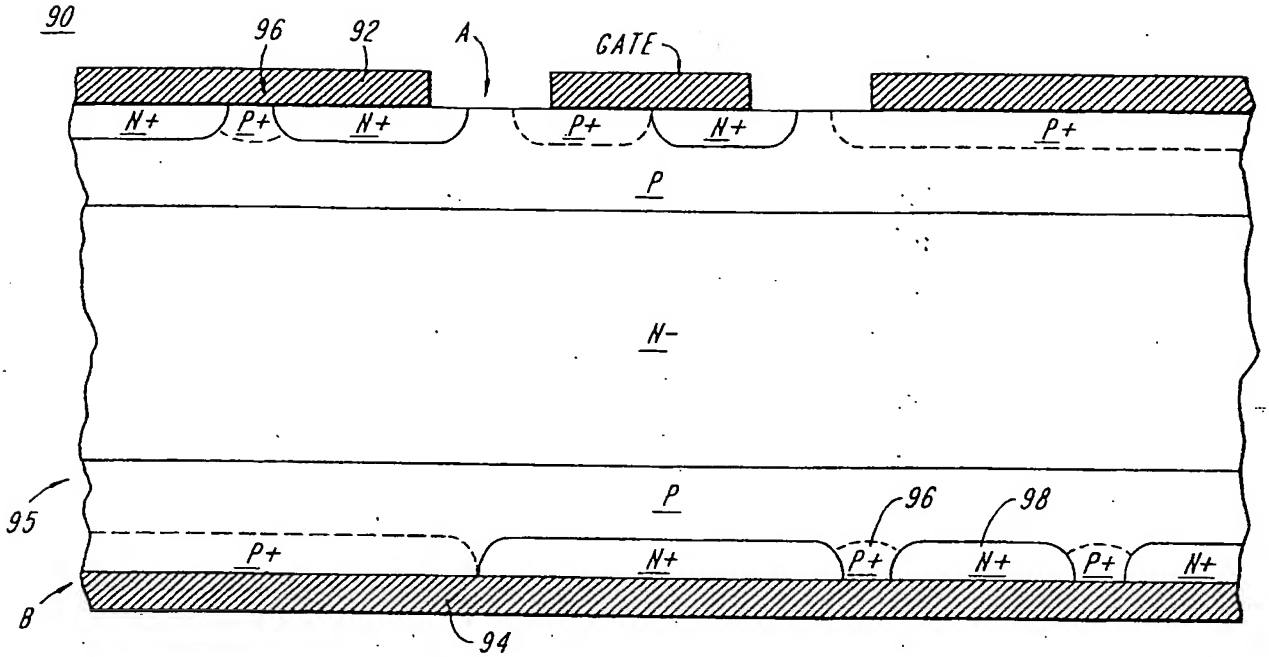

FIG. 3A
(PRIOR ART)

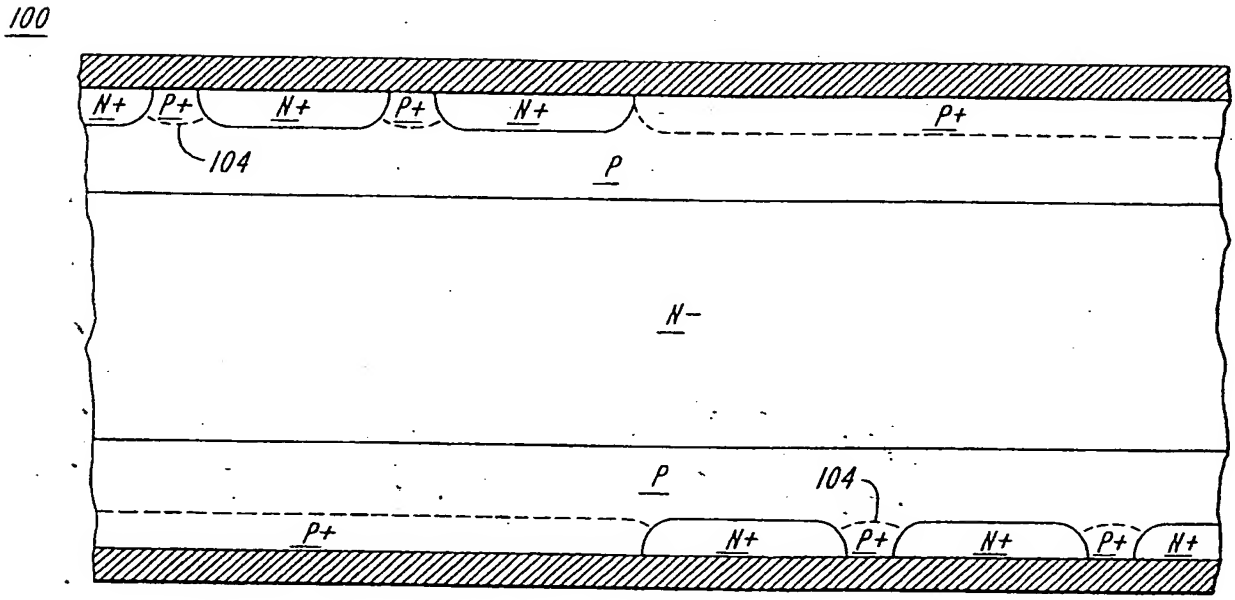

FIG. 3B
(PRIOR ART)

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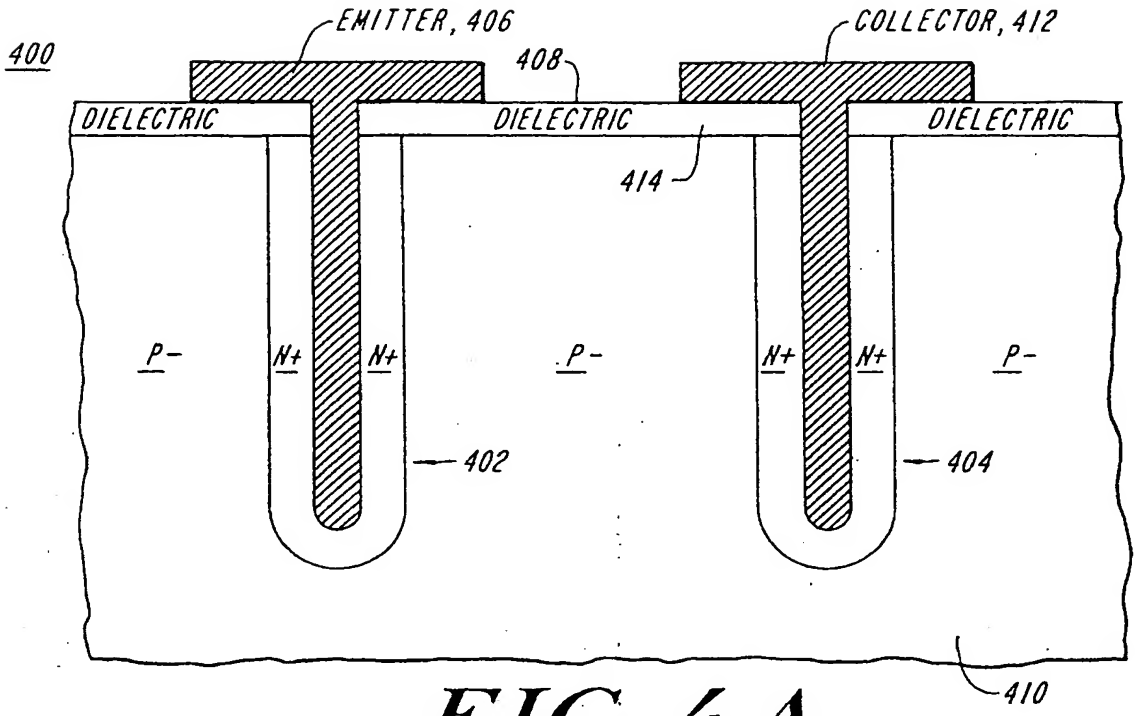

FIG. 4A

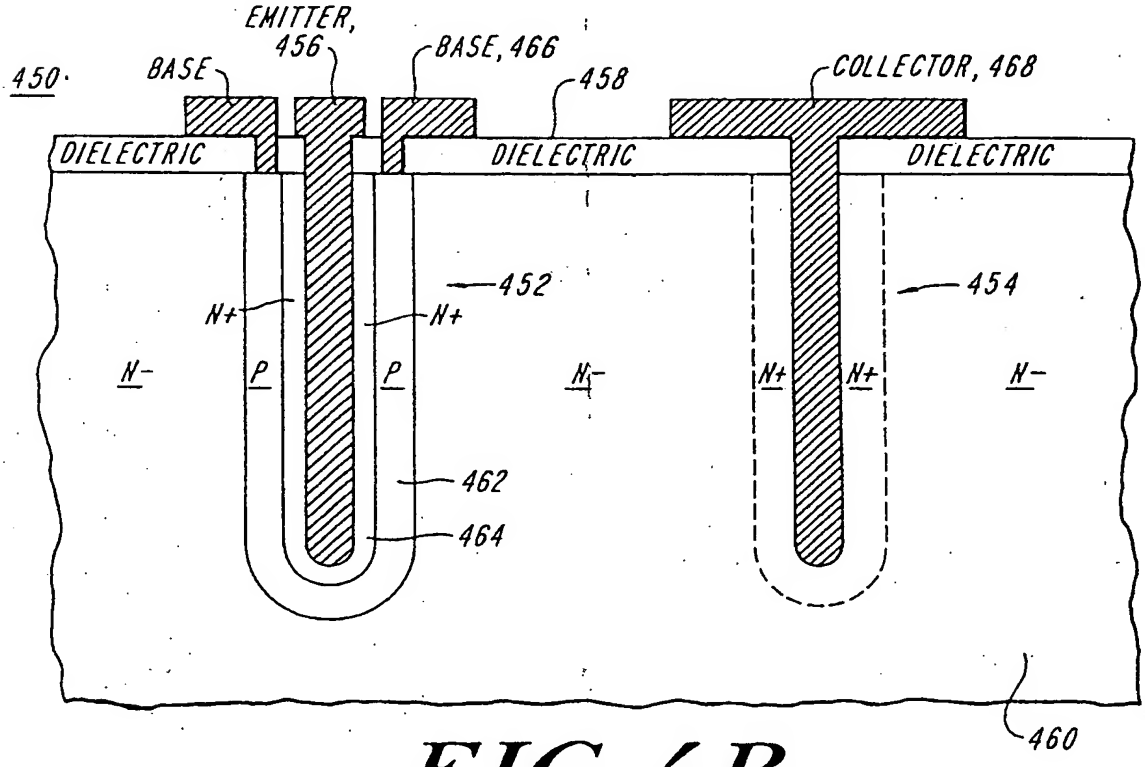

FIG. 4B

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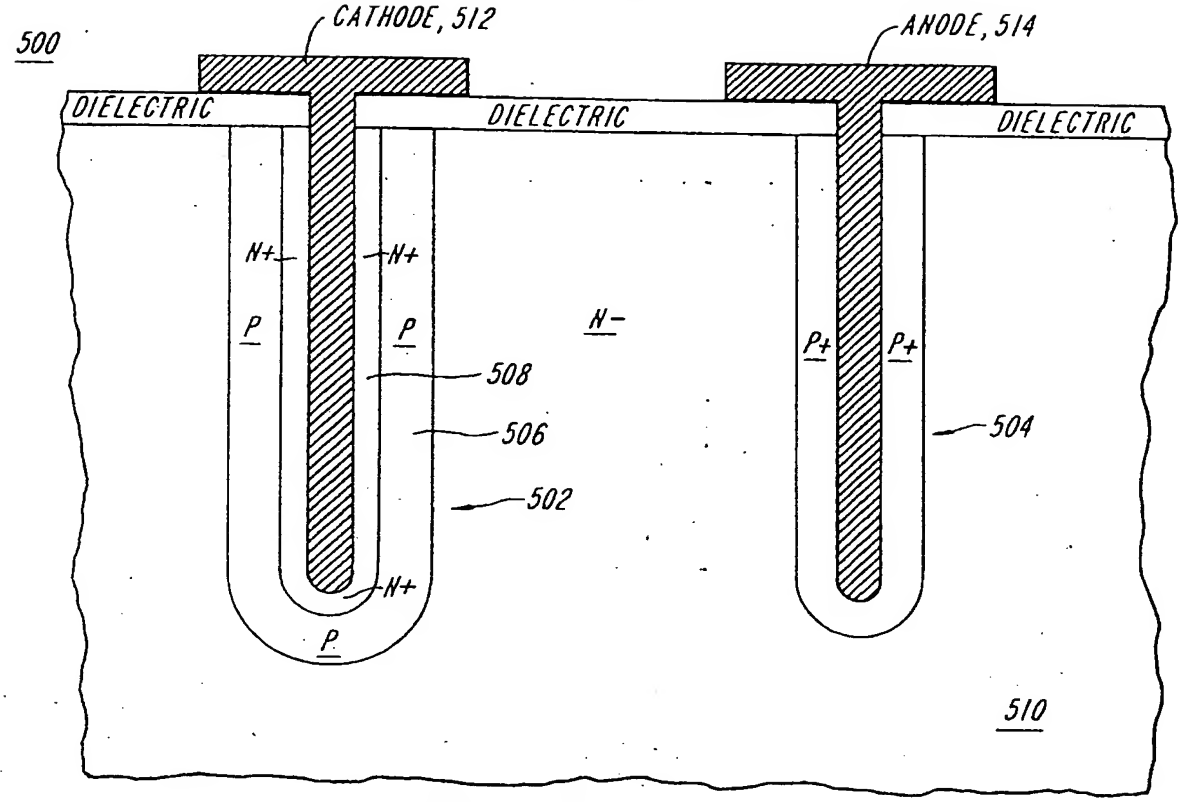

FIG. 5A

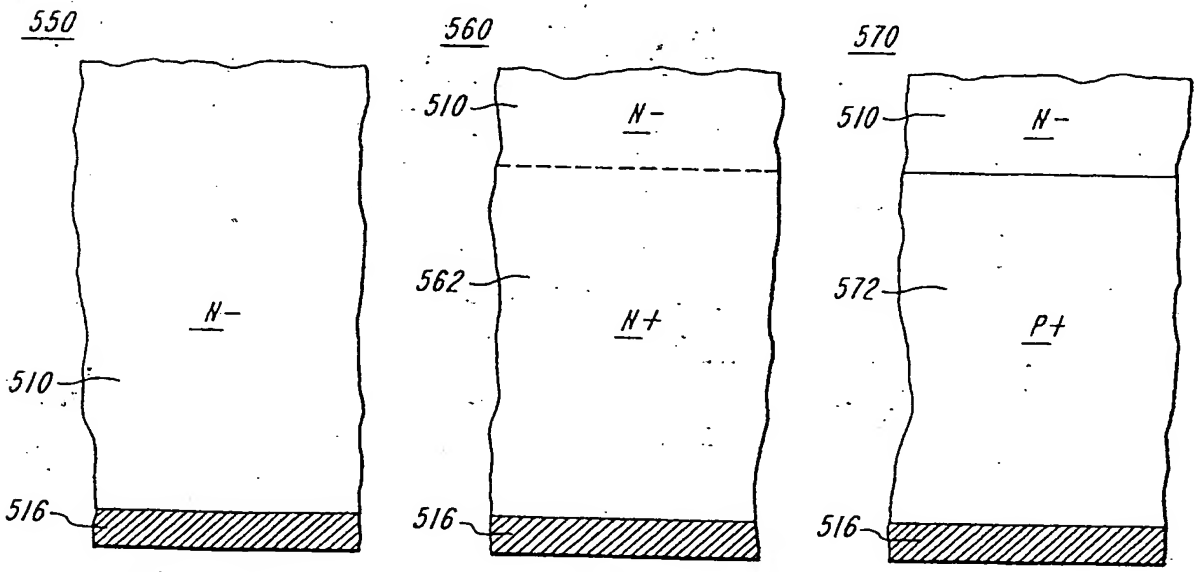

FIG. 5B

FIG. 5C

FIG. 5D

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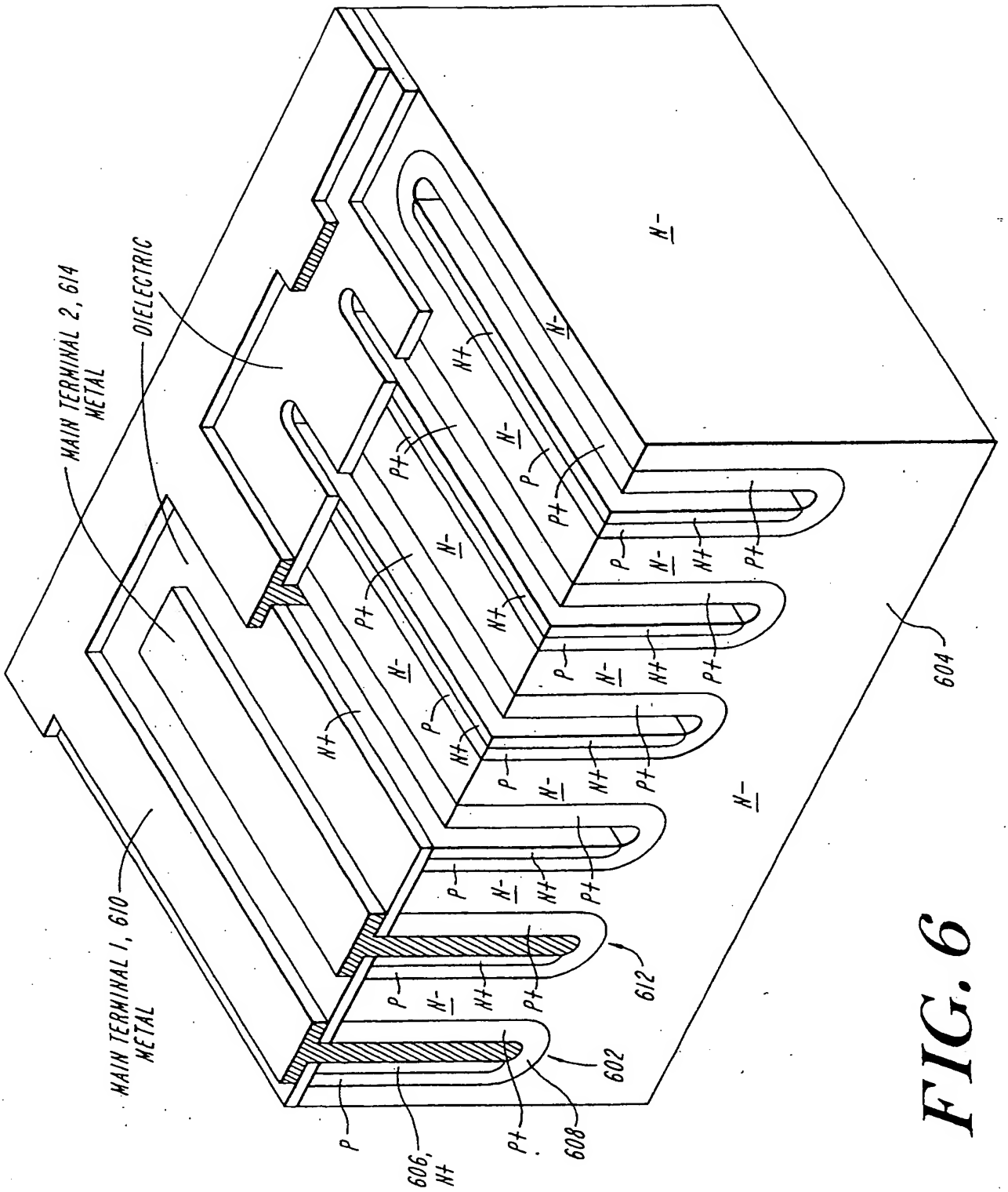

FIG. 6

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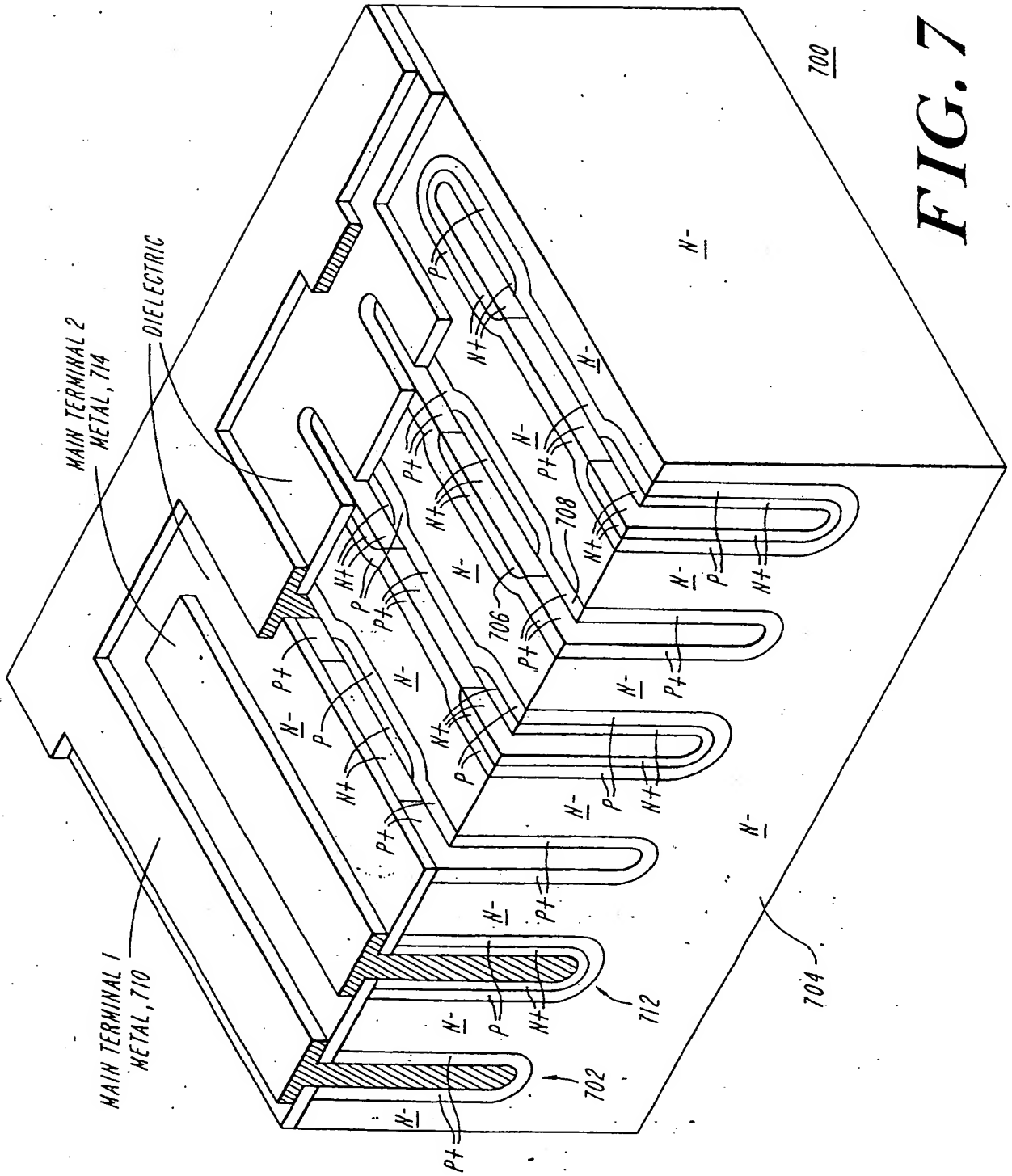


FIG. 7

SDOCID: <WO 003501BA1 >

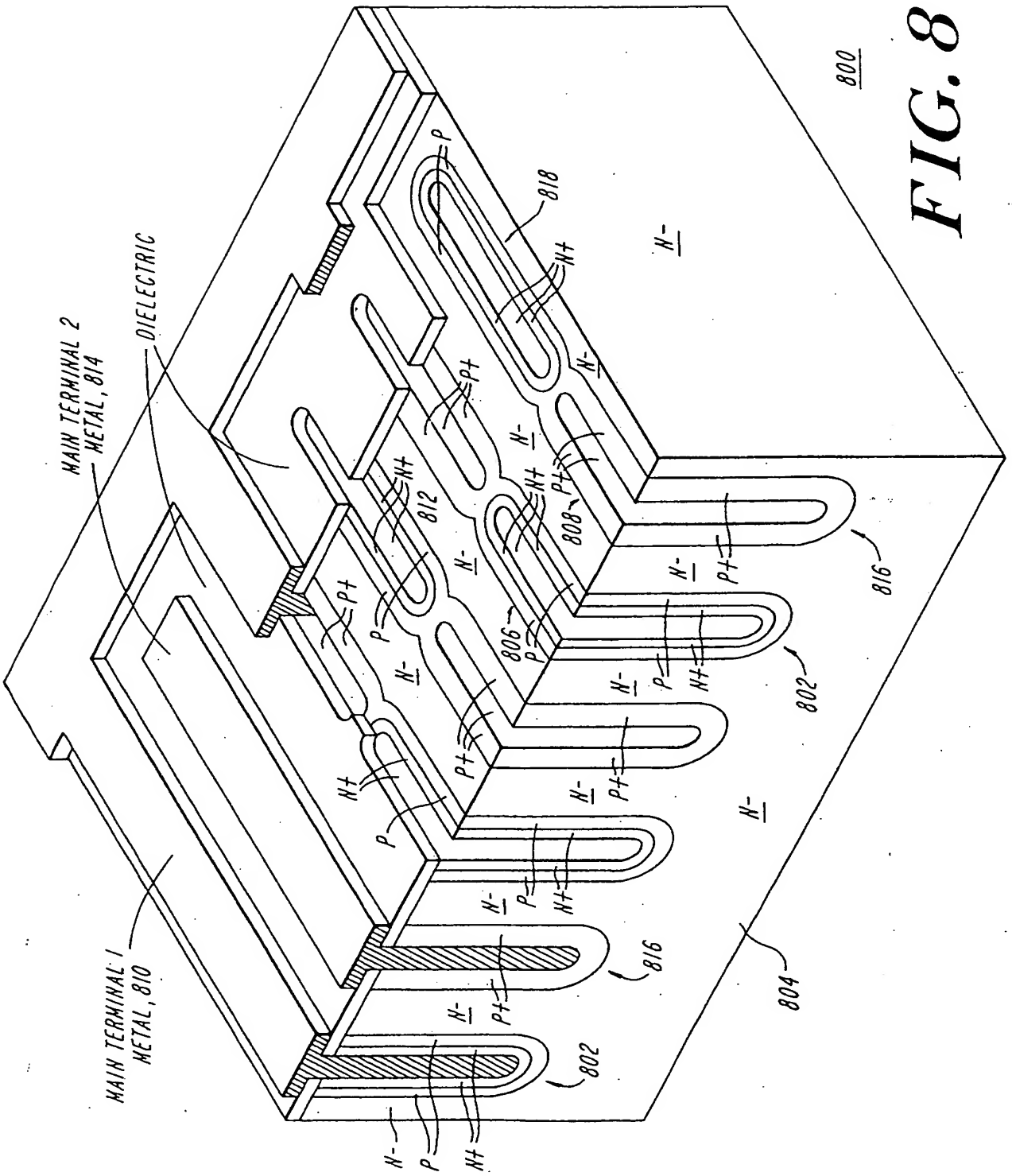
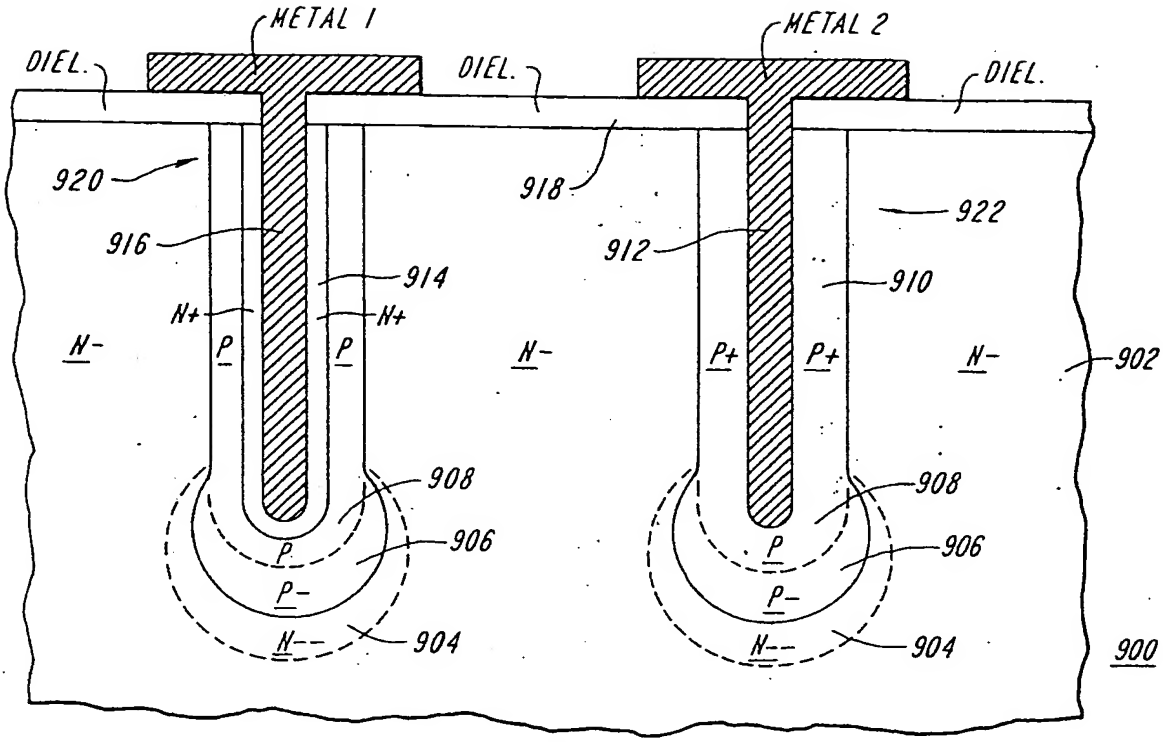


FIG. 8

NSDOCID: <WO_____0035018A1_I_>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METAL 2
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DIEL.
DIEL.
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N+
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P
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P+
P+
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908
906
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P
P
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P-
N--
N--
904
904
900

FIG. 9A

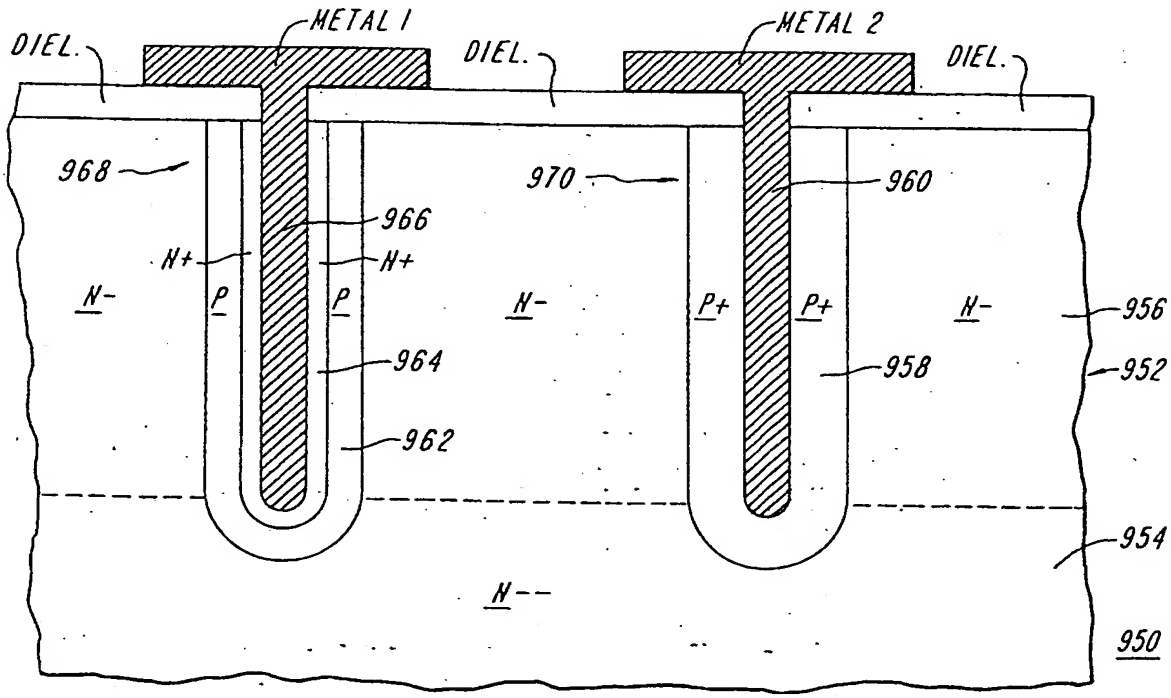
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FIG. 9B

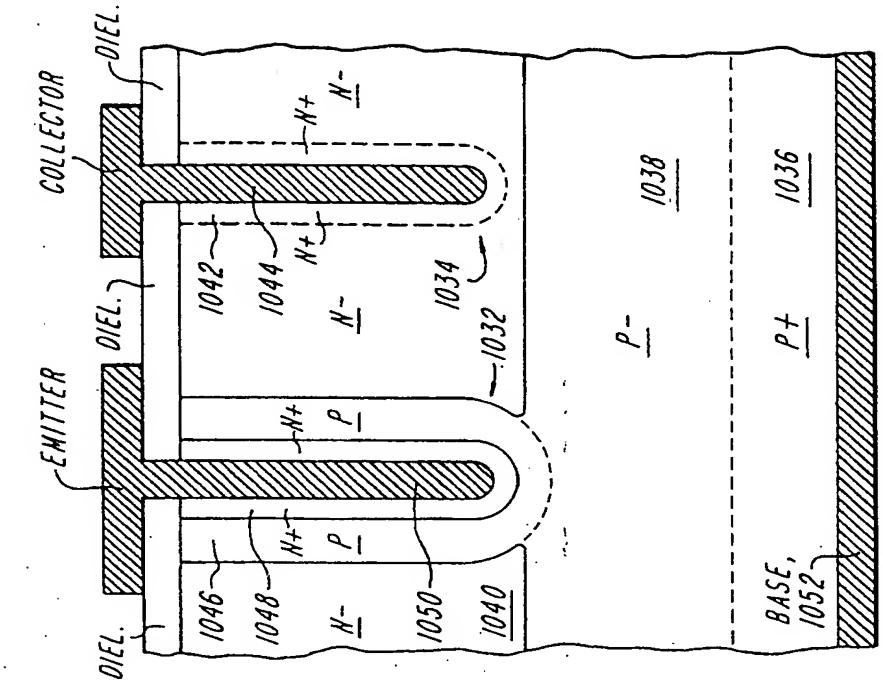

FIG. 10B

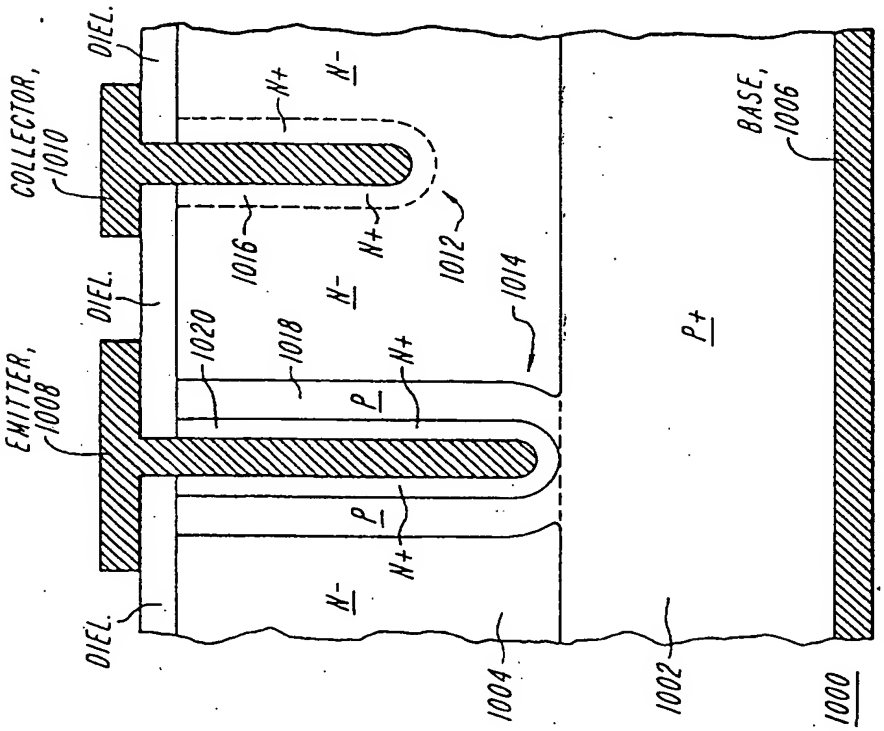

FIG. 10A

NSDOCID: <WO_____0035018A1_I_>

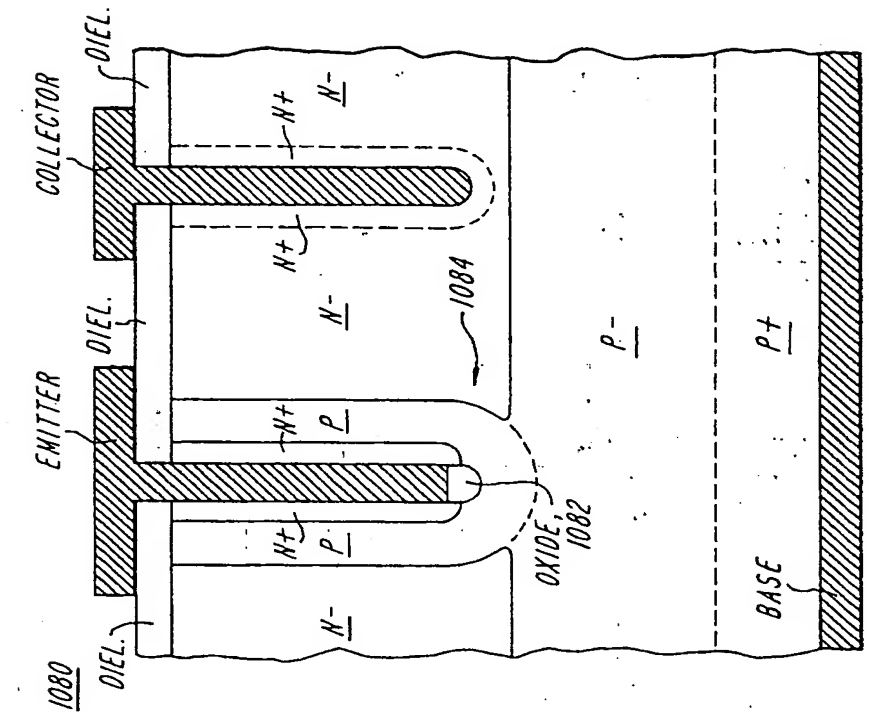

FIG. 10D

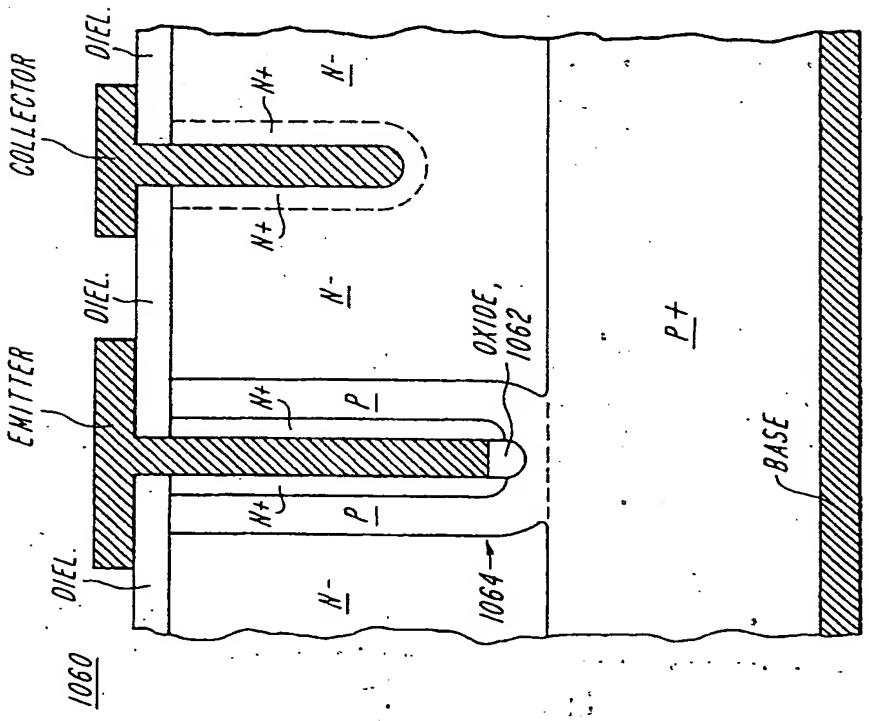

FIG. 10C

!SDOCID: <WO 0035018A1 I >

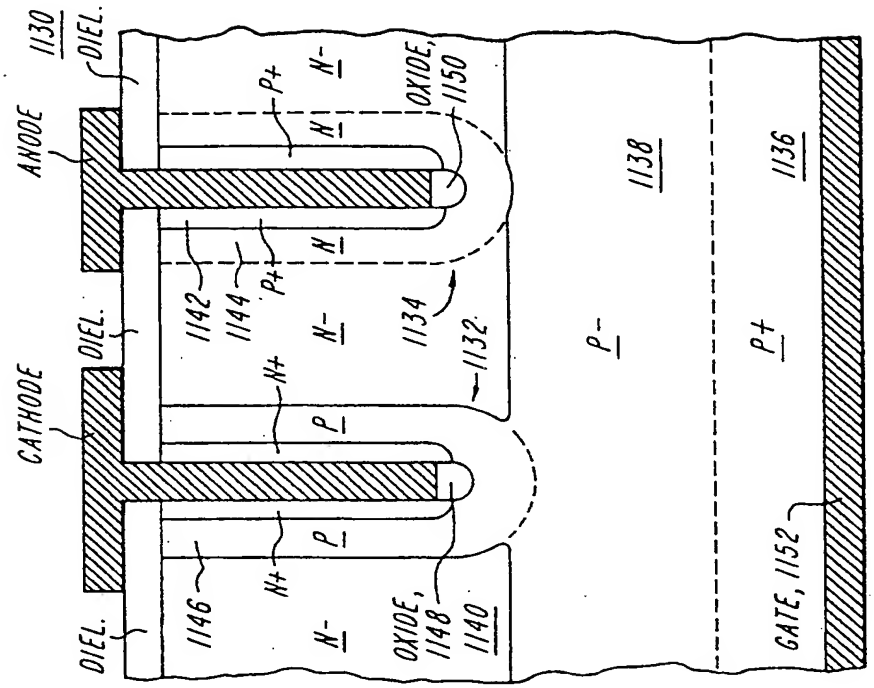

FIG. 11B

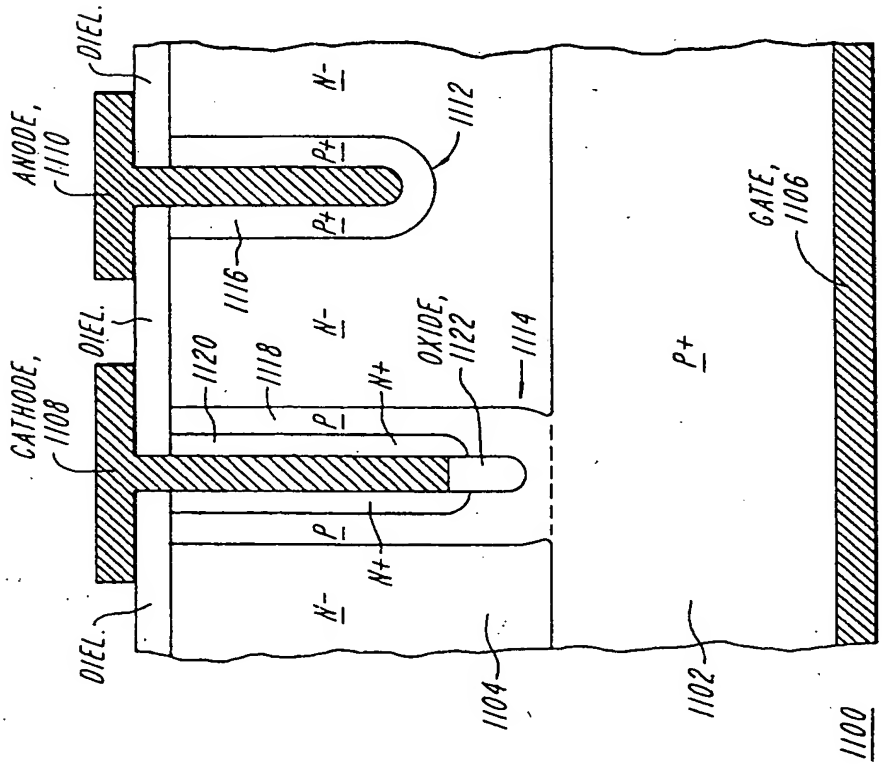

FIG. 11A

3NSDOCID: <WO_____0035018A1_I_>

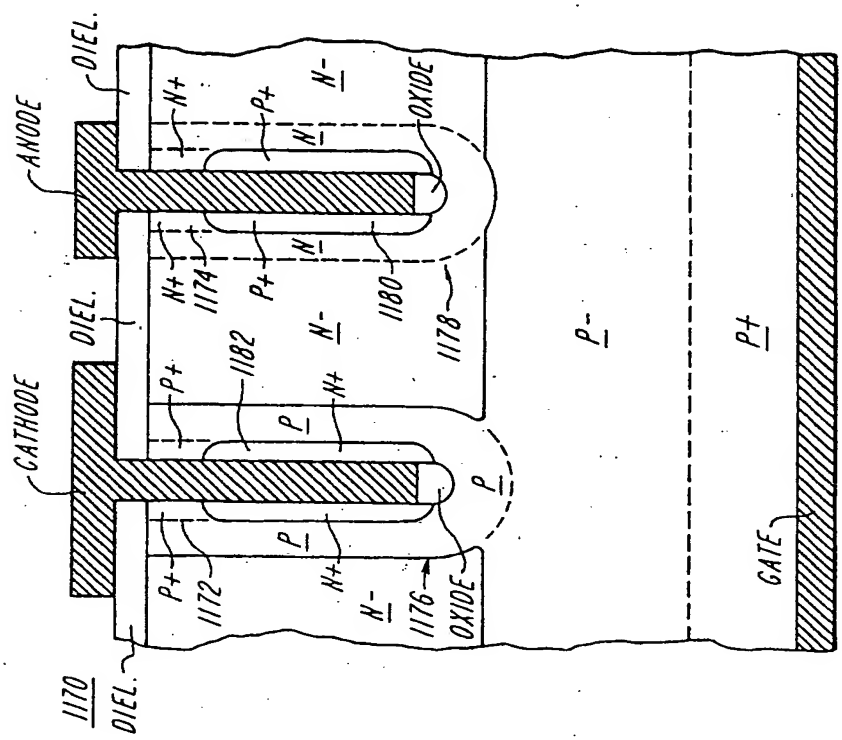

FIG. 11D

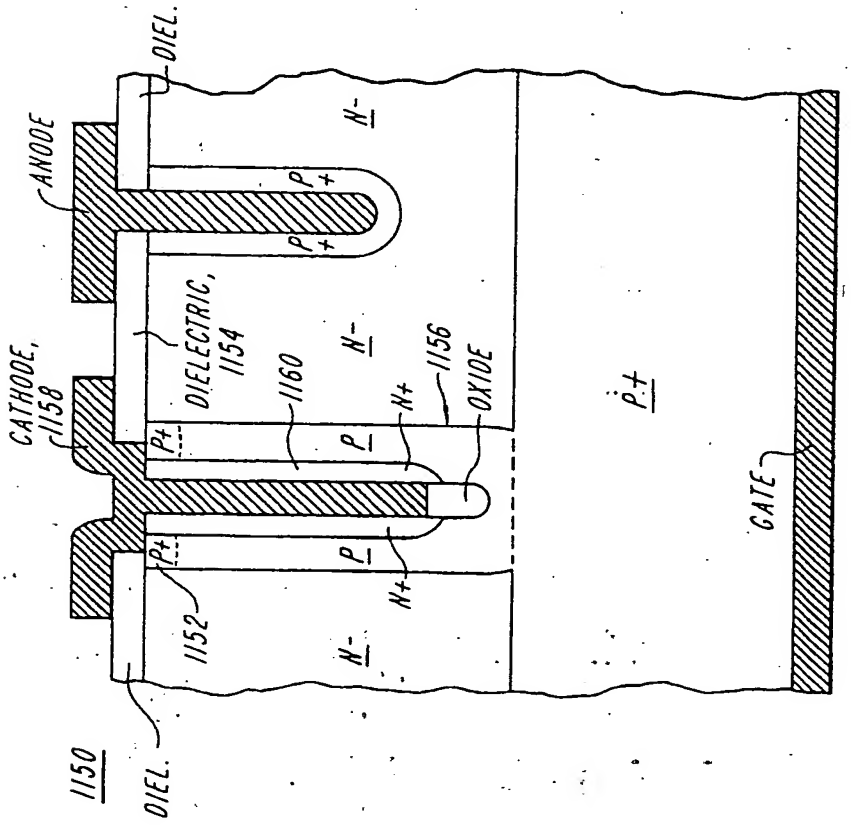

FIG. 11C

SDOCID: <WO_____0035018A1_I_>

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/29263

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 27/102, 29/41, 29/735
US CL :257/559, 586, 587, 773; 438/336, 337
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/559, 586, 587, 773; 438/336, 337

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS: trench, sidewall, metal filled, junction, lateral, bipolar. thyristor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,704,786 A (Kub) 10 November 1987 (10.11.87), entire document.	1-35
X	US 5,198,376 A (Divakaruni et al) 30 March 1993 (30.03.93), entire document.	1-35
A	US 4,749,661 A (Bower) 07 June 1988 (07.06.88), entire document.	1-35
A	US 4,795,721 A (Bower et al) 03 January 1989 (03.01.89), entire document.	1-35
A	US 4,733,287 A (Bower) 22 March 1988 (22.03.88), entire document.	1-35

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 23 FEBRUARY 2000	Date of mailing of the international search report 25 APR 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DAVID B. HARDY Telephone No. (703) 308-4092

Form PCT/ISA/210 (second sheet)(July 1992)★

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